# Vikhram Vilasur Swaminathan

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## Education

University of Illinois at Urbana-Champaign Ph.D., Mechanical Engineering (Mavis MF3 Fellowship) M.S., Mechanical Engineering

National Institute of Technology

B.Tech., Mechanical Engineering (Gold Medal & First Class with Distinction Honors)

## **Interest Areas and Expertise**

Semiconductor processing, High Aspect Ratio Etch, Micro-Electro-Mechanical Systems (MEMS), Biosensors, Microfluidics, Nanofluidics, Nanofluidics, Nanofluidics, Water Purification and Microscale Power Sources.

## Skills

**Microfabrication:** high aspect-ratio dry etch (RIE & DRIE), wet etch, photolithography, evaporation & sputter deposition, electrodeposition, atomic layer deposition, wafer/chip bonding, transfer lithography, MACEtch, PDMS molding.

**Characterization:** optical/electron microscopy, semiconductor characterization, electrochemistry, thin/thick film measurements, self-assembled monolayers, surface measurements.

Solution Development: Structured problem solving (8D, Pugh methods), SPCs, DOEs, FMEA.

Programming: MATLAB, Origin, JMP, LATEX, GIMP, ImageJ, MS Office

CAE Tools: COMSOL, ABAQUS/CAE, dw-2000, Pro/E, Autodesk Inventor, AutoCAD

## Honors and Distinctions

First Place among Oral Presentations at the Applied Materials ETch Conference	2024
Inducted as a Senior Member of the Institute of Electrical and Electronics Engineers, USA	2022
Inducted as a Member of the Royal Society of Chemistry (MRSC), UK	2021
Recognition for Competitive Differentiation: Contributions in High Aspect Ratio Etch, Lam Research Corp.	2019
Spot Awards for Contributions to Lam Core Values, Lam Research Corp.	2016/17/18
Mavis MF3 Fellowship, College of Engineering, UIUC	2011 - 13
Graduate Teacher Certificate, Center of Teaching Excellence, UIUC	2013
Featured in List of Teachers Ranked Outstanding/Excellent (6 semesters), UIUC	2010-15
Overall Outstanding Student: RECAL Alumni Association Award, NITT	2006
Convocation Gold Medalist in Mechanical Engineering, NITT	2006
Best Outgoing Student in Mechanical Engineering: RECAL Alumni Association Award, NITT	2006
JNCASR Summer Research Fellowship (among 144 students all over India)	2005
Finalist, Indian National Chemistry Olympiad (among top 58 candiates all over India)	2002

#### Experience

Process Engineer 5 (Senior Staff level) - Etch Products	July 2022 - present
Process Engineer 4 (Staff level) - Selective Removal Products Septe	mber 2020 - July 2022

• Dielectric etch, selective clean/atomic layer etching for DRAM & NAND Memory and Logic applications. Process engineering R&D and new product introductions to enable semiconductor technology roadmaps.

- Developing novel dielectric etch, highly selective etch and surface clean processes for high-aspect ratio structures.

\* Performing fundamental characterization and improvements of early stage dielectric etch tool.

\* Demonstrated highly selective and precise 3D NAND deep chop and word-line contact memory etch schemes.

Urbana, IL 2015 2011 Tiruchirappalli, India 2006

- \* Emphasis on high-throughput and versatility to etch semi-critical and back end of line features cost-effectively.
- \* Developed a highly selective bit-line contact oxide critical etch to enable N+1/N+2 DRAM technology node.
- \* Demonstrated product versatility to etch critical and non-critical features at various steps in device integration.
- Mentored, trained and oversaw junior engineers' for early-stage process development of multiple applications.
- Led the process transfer and ramp-up at high volume fab through strong cross-functional engagements and collaboration with customer and AMAT engineering, process and productivity groups.
- Pathfinding activities for engineering improvements and qualifying new product features to establish new capabilities and competitive differentiation for AMAT Etch and SRP products.
- Researched and characterized novel etch regimes that translate into new IP protection for AMAT products.

## Lam Research Corporation

Fremont, CA, USA February 2018 - September 2020 December 2015 - February 2018

Senior Process Engineer - Dielectric Etch Process Engineer - Dielectric Etch

Dielectric etch for 3D NAND & DRAM. Process engineering R&D to enable memory technology roadmaps.
 Developed etch processes to facilitate high-aspect ratio FEOL patterning of dielectric stacks.

- Facilitated process transfer and ramp-up to production at high volume fab through strong cross-functional engagements and collaboration with customer and Lam's engineering, process, productivity and deposition groups.
  - \* Enabled qualification of critical pillar etch process for 2 technology nodes for a 3D NAND etch application.
  - \* Demonstrated up to 35% improved throughput for a 3D NAND Slit etch process for 3 technology nodes.
  - \* Enabled, via pathfinding, a penetration opportunity in capacitor cell etch business for sub-50nm pitch DRAM nodes.
- Synthesized data-driven solutions to yield problems through root cause analysis of critical factors.
  - \* Implemented statistically robust solutions, with hardware kits and process tuning, for 300mm wafer uniformity.
- Demonstrated process engineering improvements and new product features to establish new capabilities and competitive differentiation for Lam products.
- Researched and characterized novel etch regimes that translated into new IP protection for Lam products.

University of Illinois at Urbana-Champaign	Urbana, IL, USA	
Postdoctoral Research Associate: Department of Bioengineering	September 2015 - November 2015	
Research Assistant: Shannon/Bashir Research Groups	April 2008 - Aug 2015	
Graduate Mentor: Illinois Scholars Undergraduate Research (ISUR) Program	August 2009 - May 2010	
Instructional Teaching Assistant: Mechanical Science and Engineering	May - August 2012	
Teaching Assistant: Laboratory, tutoring and grading	(10 semesters) August 2007 - May 2015	
• Label free conging using FET biggengeng. Adapted description techniques to eveneeme Debug geneening of FETa		

• Label-free sensing using FET biosensors. Adapted deionization techniques to overcome Debye screening of FETs.

- Developed a *transistor-in-droplet* framework for high-throughput, multiplexed detection of biomarkers using FETs.
  \* One of the first demonstrations of multiplexing & large statistical measurements with (*million-pixel*) FET biosensors.
- Fabricated and extensively characterized nanotextured microelectrodes for simultaneous desalting and sensing.
  \* Adapted analytical models for double-layer screening of highly saline media, with experimental validation and surface treatment of the microelectrodes to maximize desalting performance.
  - \* Demonstrated a novel capability to bias a FET sensor using the microelectrodes during desalting.
- Collaborated with a diagnostics major and a semiconductor foundry. Secured patent applications.
- Microfluidic separation of sub-micron colloids. Developed electrostatic methods for enhanced dielectrophoresis.
  - Microfabricated high aspect-ratio interdigitated electrode arrays to capture colloidal nanoparticles in microchannels.
  - Simulated and experimentally verified the enhanced separation effects of mixed AC/DC dielectrophoresis.
  - Demonstrated multiple schemes to capture nanoparticles based on salinity for upstream use in reverse osmosis systems.
- Hierarchical nanostructures in silicon. Nanofabricated structures with tunable surface geometry and hierarchy.
  - Developed a one-mask microfabrication flow to etch re-entrant features with out-of-plane nanopillars in silicon.
  - Demonstrated an extremely hydrophobic surface with  ${\sim}171^\circ$  water contact angle and  ${<}1^\circ$  sliding angle.
- Fuel cell PowerMEMS. Integrated hydrogen sources and fuel cells into a PowerMEMS using microfabrication methods.
  - Designed, fabricated & characterized a prototype micro fuel cell passive with microfluidic self-regulation scheme.
  - Demonstrated ultra-high capacity of 200 Whr/L energy density and >300 W/L power density.
    - \* One of the world's smallest Fuel Cells, and the highest energy/power density demonstration of a PowerMEMS.

# Indian Institute of Science

Bangalore, India

JNCASR Summer Research Fellow and Project Assistant
 May - July 2005, October - December 2006
 Compliant MEMS synthesis. Designed a bistable MEMS switch using four-bar mechanisms, torsional joints & electro-thermal-compliant (ETC) microactuators, and simulated their coupled mechanics using ABAQUS finite element analysis to synthesize optimized prototype structures.

## **Patent Publications**

- R. Bashir, V.V. Swaminathan, B. Reddy, Jr., E. Salm & C. Duarte-Guevara, "Label Free Analyte Detection by Electronic Desalting and Field Effect Transistors", US Patent #10,527,579, USPTO, issued 7 Jan. 2020.
- 2. N. Dole, V.V. Swaminathan, B. Jiang & M. Wong, "Multi-state rf pulsing to control mask shape and breaking selectivity versus process margin trade-off", US Application #2022-0285130 A1, USPTO, filed 2019 (patent pending).

## **Book Chapters**

- 1. N. Dole et al., "Corona Treatment of Polymer Surfaces to Enhance Adhesion", Polymer Surface Modification to Enhance Adhesion: Techniques and Applications: K.L. Mittal & A. Netravali (eds.), Scrivener Publishing (Wiley), USA, 2024.
- 2. D.P.R Thanu et al., "Use of Surfactants in Acoustic Cleaning", Surfactants in Precision Cleaning: Removal of Contaminants at the Micro and Nanoscale: R. Kohli & K.L. Mittal (eds.), Elsevier, Netherlands, 2021.
- 3. V.V. Swaminathan et al., "Ionic Transport in Nanocapillary Membrane Systems", Nanotechnology for Sustainable Development: M.S. Diallo, N.A. Fromer, M.S. Jhon (eds.), Springer International Publishing, Switzerland, 2014.

## Selected Journal Publications

- 1. V.V. Swaminathan et al., "Electronic desalting for controlling the ionic environment in droplet-based biosensing platforms", Applied Physics Letters, vol. 106, 2015, pp. 053105.
- 2. V.V. Swaminathan et al., "Enhanced sub-micron colloidal particle separation with interdigitated microelectrode arrays using mixed AC/DC dielectrophoretic scheme", *Biomedical Microdevices*, vol. 17, 2015, pp. 29.
- 3. H. Hu, V.V. Swaminathan et al., "Hierarchically Structured Re-entrant Microstructures for Superhydrophobic Surfaces with Extremely Low Hysteresis", Journal of Micromechanics and Microengineering, vol. 24, 2014, 095023 (co-first author).
- 4. V.V. Swaminathan et al., "Ionic Transport in Nanocapillary Membrane Systems", Journal of Nanoparticle Research: special issue on Nanotechnology for Sustainable Development, vol. 14, 2012, pp. 951-65.
- 5. V.V. Swaminathan et al., "Integrated micro fuel cell with on-demand hydrogen production and passive control MEMS", Microfluidics & Nanofluidics, vol.12, 2012, pp. 735-49.
- C. Duarte-Guevara, V.V. Swaminathan et al., "Characterization of a 1024 x 1024 DG-BioFET platform", Sensors and Actuators B: Chemical, vol. 250, 2017, pp. 100-110.

#### Service and Leadership

- Memberships in Professional and Scientific Societies: IEEE and RSC.
- Peer reviewer for AIP Advances Journal and The Journal of Sol-Gel Science and Technology.
- Finisher at the Chicago Full Marathon, raised funds for Asha for Education charity, 2009. Team Asha Marathon Coordinator for Asha Urbana-Champaign Chapter, 2010-12.
- President of *Balls By Picasso*, the English Literary Society of NITT, 2005-06. Literary Championships representing NITT at IIMB and JIPMER.
- Editor-in-Chief of Mechanical Engineering Department, 2005-06, NITT.